AMENDMENTS TO THE CLAIMS:

This listing of the claims replaces all prior versions and listing of the claims in the present application.

Listing of Claims:

1. (previously presented) A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

MOS transistors which are disposed in said substrate and which include first gate insulating films; and

an MOS type varactor element which is disposed in said substrate and which includes a second gate insulating film, a gate electrode and a second conductivity type well, wherein said second gate insulating film, said gate electrode and second conductivity type well are a variable capacitor,

a thickness of said second gate insulating film being thinner than the thinnest gate insulating film among said first gate insulating films of said MOS transistors.

2. (original) A semiconductor integrated circuit device according to Claim 1, wherein a maximum gate voltage applied to said MOS type varactor element is lower than a maximum gate voltage applied to said MOS transistors.

3. (original) A semiconductor integrated circuit device according to Claim 1, wherein said substrate is a semiconductor substrate.

4. (original) A semiconductor integrated circuit device according to Claim 2, wherein said substrate is a semiconductor substrate.

5. (previously presented) A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

plural MOS transistors which are disposed in said substrate and which include gate insulating films, said MOS transistors not being part of a varactor; and

an MOS type varactor in said substrate and spaced from said plural MOS transistors and which includes a gate insulating film, a thickness of said gate insulating film of said varactor being thinner than the thinnest gate insulating film among said gate insulating films of said plural MOS transistors, said varactor including a second conductivity type well in an upper surface of said first conductivity type substrate, two first conductivity type diffusion regions in an upper surface of said second conductivity type well, said two diffusion regions having higher impurity concentrations than said well and being directly connected to a same ground terminal, said gate insulating film of said varactor being on said upper surface of said well between said two diffusion regions, and a gate electrode on said gate insulating film between said two diffusion regions.

6. (previously presented) The device of claim 5, wherein said gate insulating film of said varactor and said gate

insulating films of said plural MOS transistors are at a same level of the device.

7. (previously presented) The device of claim 5, wherein the thickness of said gate insulating film of said varactor is about three quarters of a thickness of said gate insulating films of said plural MOS transistors.

8. (previously presented) The device of claim 7, wherein the thickness of said gate insulating film of said varactor is about 6 nm and the thickness of said gate insulating films of said plural MOS transistors is about 8 nm.

9. (previously presented) The device of claim 5, wherein said plural MOS transistors include an N-channel MOS transistor and a P-channel MOS transistor.

10. (previously presented) The device of claim 1, wherein said second gate insulating film of said varactor element and said first gate insulating films of said MOS transistors are at a same level of the device.

11. (previously presented) The device of claim 1, wherein the thickness of said second gate insulating film of said varactor element is about three quarters of a thickness of said first gate insulating films of said MOS transistors.

12. (previously presented) The device of claim 11, wherein the thickness of said second gate insulating film of said varactor element is about 6 nm and the thickness of said first gate insulating films of said MOS transistors is about 8 nm.

13. (previously presented) The device of claim 1, wherein said MOS transistors are spaced from said varactor element and include an N-channel MOS transistor and a P-channel MOS transistor.

14. (currently amended) The device of claim 9, wherein the first conductivity type is a P type and the second conductivity type is N type, and further comprising an N^+ diffusion region placed in an area separated from directly under the gate electrode and the [[P^+]] diffusion regions in the surface of the [[N]] well, and a P^+ diffusion region placed at a part of an area where the [[N]] well is not disposed in the upper surface of the ~~P type~~ substrate.

15. (previously presented) The semiconductor integrated circuit device according to claim 1, wherein said MOS type varactor element further includes a second conductivity type diffusion layer connected to said second conductivity type well.

16. (previously presented) The semiconductor integrated circuit device according to claim 15, wherein said second conductivity type diffusion layer of said MOS type varactor element is adjacent to a side of said gate electrode.

17. (currently amended) ~~The semiconductor integrated circuit device according to claim 15,~~ A semiconductor integrated circuit device comprising:

a first conductivity type substrate;

MOS transistors which are disposed in said substrate and which include first gate insulating films; and

an MOS type varactor element which is disposed in said substrate and which includes a second gate insulating film, a gate electrode and a second conductivity type well, wherein said second gate insulating film, said gate electrode and second conductivity type well are a variable capacitor,

a thickness of said second gate insulating film being thinner than the thinnest gate insulating film among said first gate insulating films of said MOS transistors,

wherein said MOS type varactor element further includes a second conductivity type diffusion layer connected to said second conductivity type well, and

wherein said second conductivity type diffusion layer of said MOS type varactor element is adjacent to both sides of said gate electrode.

18. (previously presented) The semiconductor integrated circuit device according to claim 17, wherein a potential of said second conductivity type diffusion layer adjacent to one side of said gate electrode is substantially equal to a potential of said second conductivity type diffusion layer adjacent to another side of said gate electrode.

19. (previously presented) The semiconductor integrated circuit device according to claim 15, wherein said MOS type varactor element further includes a first conductivity type

diffusion layer, and said first conductivity type diffusion layer is adjacent to a side of said gate electrode.

20. (previously presented) The semiconductor integrated circuit device according to claim 15, wherein said MOS type varactor element further includes a first conductivity type diffusion layer, and said first conductivity type diffusion layer of said MOS type varactor element is adjacent to both sides of said gate electrode.

21. (previously presented) The semiconductor integrated circuit device according to claim 20, wherein a potential of said first conductivity type diffusion layer adjacent to one side of said gate electrode is substantially equal to a potential of said first conductivity type diffusion layer adjacent to another side of said gate electrode.

22. (previously presented) The semiconductor integrated circuit device according to claim 19, wherein a potential of said first conductivity type diffusion layer adjacent to a side of said gate electrode is ground potential.